Remarks

Claims 1-7 are currently pending in the patent application. In the discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

In the Final Office Action dated June 13, 2008, the following rejections are indicated: claims 1-6 stand rejected under 35 U.S.C. § 102(b) over the Watanabe reference (U.S. Patent No. 5,721,091); and claim 7 stands rejected under 35 U.S.C. § 103 (a) in view of the Watanabe reference. Applicant respectfully traverses these rejections.

The § 102(b) and § 103(a) rejections are improper because the Watanabe reference fails to teach or suggest all the features recited in Applicant's claims. In particular, Applicant submits that Watanabe appears to disclose none of the claimed features relevant to wafer dicing, including those features relating to exposure fields, lattice fields in the exposure fields, an IC in each lattice field, dicing paths, control fields that do not reside in any dicing paths, and at least one control module including an optical control module in place of a preset number of lattice fields.

As understood by Applicant, the Watanabe reference is unrelated to the wafer dicing subject matter recited in Applicant's claims. Instead, Watanabe teaches a resist composition that prevents charging during certain processing steps such as ion implantation. As explained by Watanabe, misalignment can occur during resist-based patterning processes when the resist material takes on an electrical charge (*see, e.g.*, Col. 2:58-66). The cited portions of Watanabe, and in particular Figs. 7A-7E, discuss evaluation of charge-up prevention in which alignment marks are provided for the purpose of checking for any misregistration or other dimensional errors after exposing the photoresist layer to an electron beam (*see, e.g.*, Col. 11:65 through Col. 12:18). Applicant finds nothing in the Watanabe reference that mentions any application to dicing operations, much less that teaches or suggests that the disclosed alignment marks could somehow be construed as optical control modules that replace a present number of IC-containing lattice fields that are separated along dicing paths, as claimed.

For at least these reasons, Applicant submits that the rejections based on the Watanabe reference are improper and requests their reconsideration and withdrawal.

Applicant further requests that the finality of the Final Office Action be withdrawn. In accordance with M.P.E.P. § 706.07(a), a final rejection is improper on a second Office Action when the Examiner introduces a new ground of rejection that is neither necessitated by Applicant's amendment, nor based on information submitted in an information disclosure statement filed during the period set forth in 37 C.F.R. 1.97(c). In this case, the Examiner predicated the final rejection on the new ground of rejection being necessitated by Applicant's amendment. Applicant submits, however, that the amendment presented in Applicant's Response of March 12, 2008 was for clarification purposes and did not alter the intended scope of the claims. In particular, the added phrase, "such that the control module fields do not reside in any of the dicing paths," merely recites what one of skill in the art would have already understood from Applicant's description. For example, the control module fields are disclosed and claimed to be contained in the exposure fields, and one of skill in the art would understand that the boundaries of the exposure fields are defined by the dicing paths. As such, the exposure fields, and therefore the control module fields, cannot reside in any of the dicing paths. For these reasons, Applicant submits that the scope of the claims has not been altered, and therefore that the new ground of rejection cannot have been necessitated by Applicant's amendment. Withdrawal of the finality of the rejection is therefore requested.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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